

ICs for Communications

Mini IOM-2 Controller
MICO

PEF 2015 Version 1.1

Product Overview 03.97

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Previous Version:Product Overview 03.96		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
5	5	IOM-2 interface supporting 8 IOM-2 channels (old version: 4)
-	6	Pinning diagram
10	11	µP interface description updated
10	11	Special functions extendend

Edition 03.97

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1 Overview

The Mini IOM-2 Controller MICO (PEF 2015) is an interface controller optimized for small line card applications or Intelligent NTs. It is derived from the EPIC core. The MICO supports up to 16 analog subscribers (up to 8 using the SLICOFI) or up to 8 ISDN-BA subscribers.

The MICO is used as an interface device on linecards between the subscriber circuits and the network. Therefore it provides one IOM-2 interface for connection of up to 8 ISDN-BA subscribers or up to 16 analog subscribers (up to 8 using the SLICOFI). The MICO also provides one PCM interface for connection to the main system. Additionally the MICO is used to control the subscriber circuits via the C/I and monitor channel as specified in the IOM-2 specification. A parallel μ P interface is provided for device programming.

Furthermore the MICO contains a nonblocking switching unit with a flexible time slot assignment between the IOM-2 and the PCM interface.

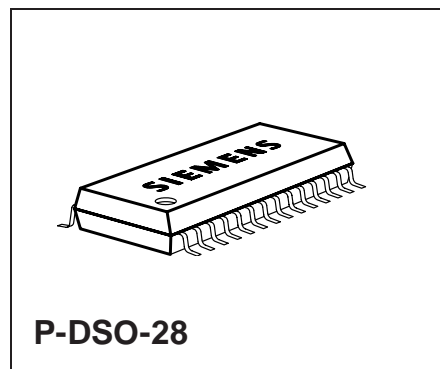
The MICO may substitute the EPIC (PEB 2055) or EPIC-S (PEB 2054) in applications that deal with a maximum number of 8 ISDN or 16 analog (8 using the SLICOFI) subscribers connected via one IOM-2 port.

The MICO will be fabricated using SIEMENS advanced CMOS technology and will be available in a P-DSO-28 package.

1.1 Features

Functions

- Interface controller between IOM-2 and PCM for up to 8 ISDN-BA or 16 analog subscribers (up to 8 analog subscribers using the SLICOFI)
- B-channel (64 kbit/s) and D-channel (16 kbit/s) switching
- Configurable Interface (1 port)
 - Configurable for IOM-, SLD- and PCM-applications
 - Programmable clock shift
 - Single or double data clock
- PCM interface (1 port)
 - Freely programmable time slot assignment to up to 128 PCM time slots
 - Tristate control signal for external driver
 - Single or double data clock
- C/I-channel Handler with a 9-Byte FIFO
- Buffered Monitor Handler with a 16-Byte FIFO
- Data rate adaption by a programmable PCM clock rate up to 8.192 MHz (single or double data rate)
- 7-bit hardware timer



General

- Siemens/Intel or Motorola type μ P interface
- Supply Voltage: 5 V
- Extended temperature range -40°C to +85°C
- P-DSO-28 package

Type	Ordering Code	Package
PEF 2015		P-DSO-28

1.2 Pinning Diagram

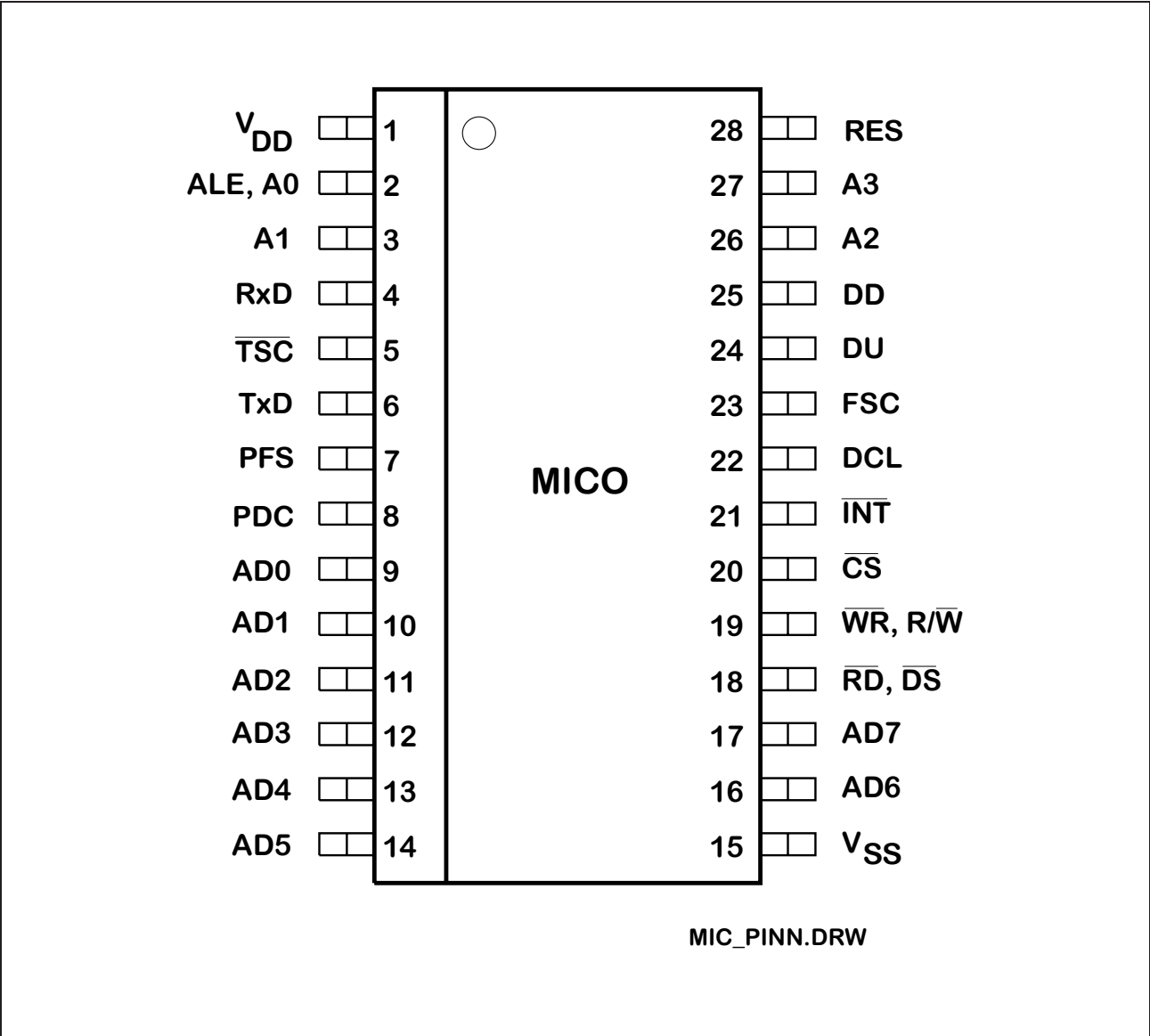


Figure 1
Pinning Diagram

1.3 Logic Symbol

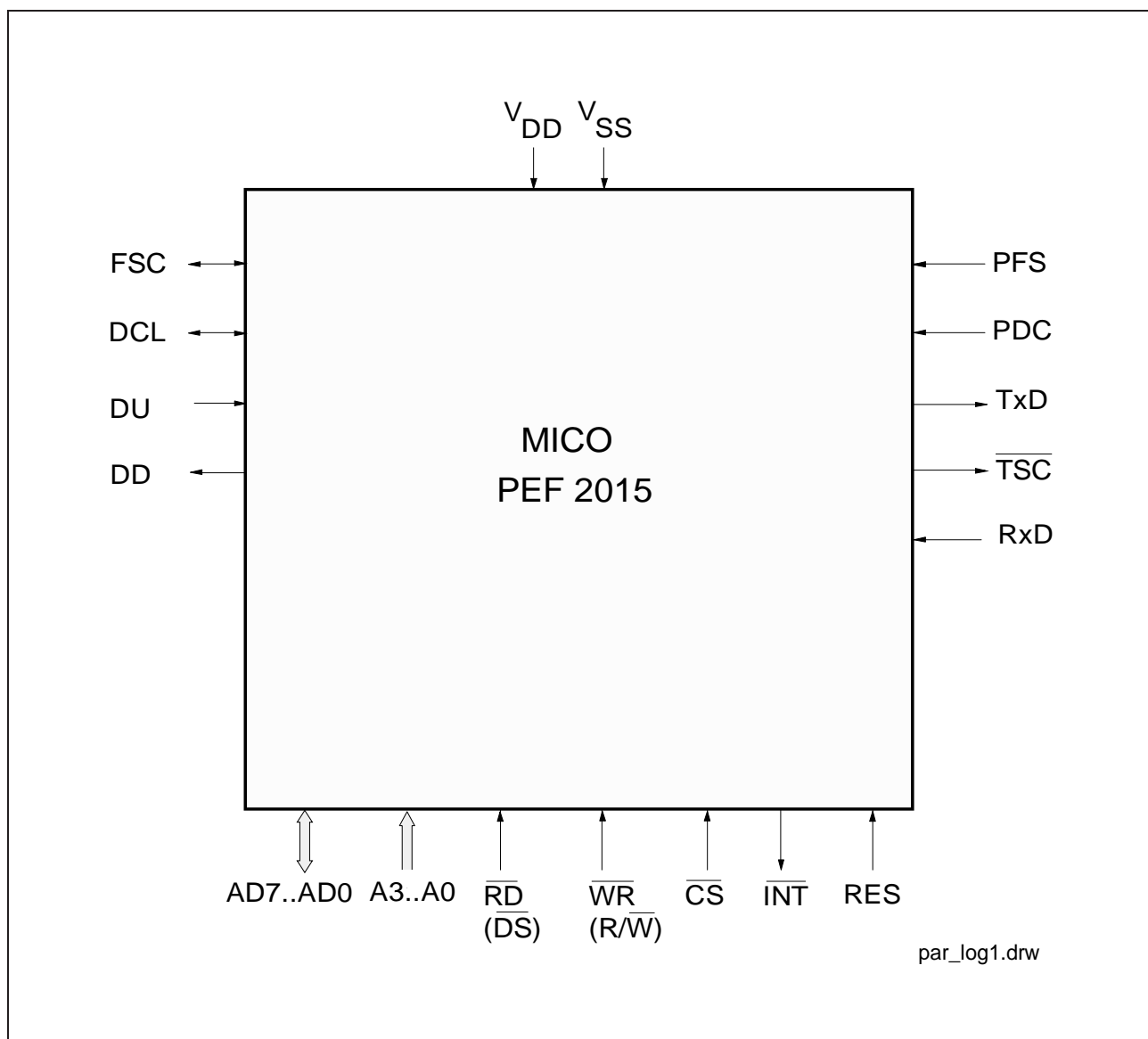


Figure 2
Logic Symbol

1.4 Functional Block Diagram

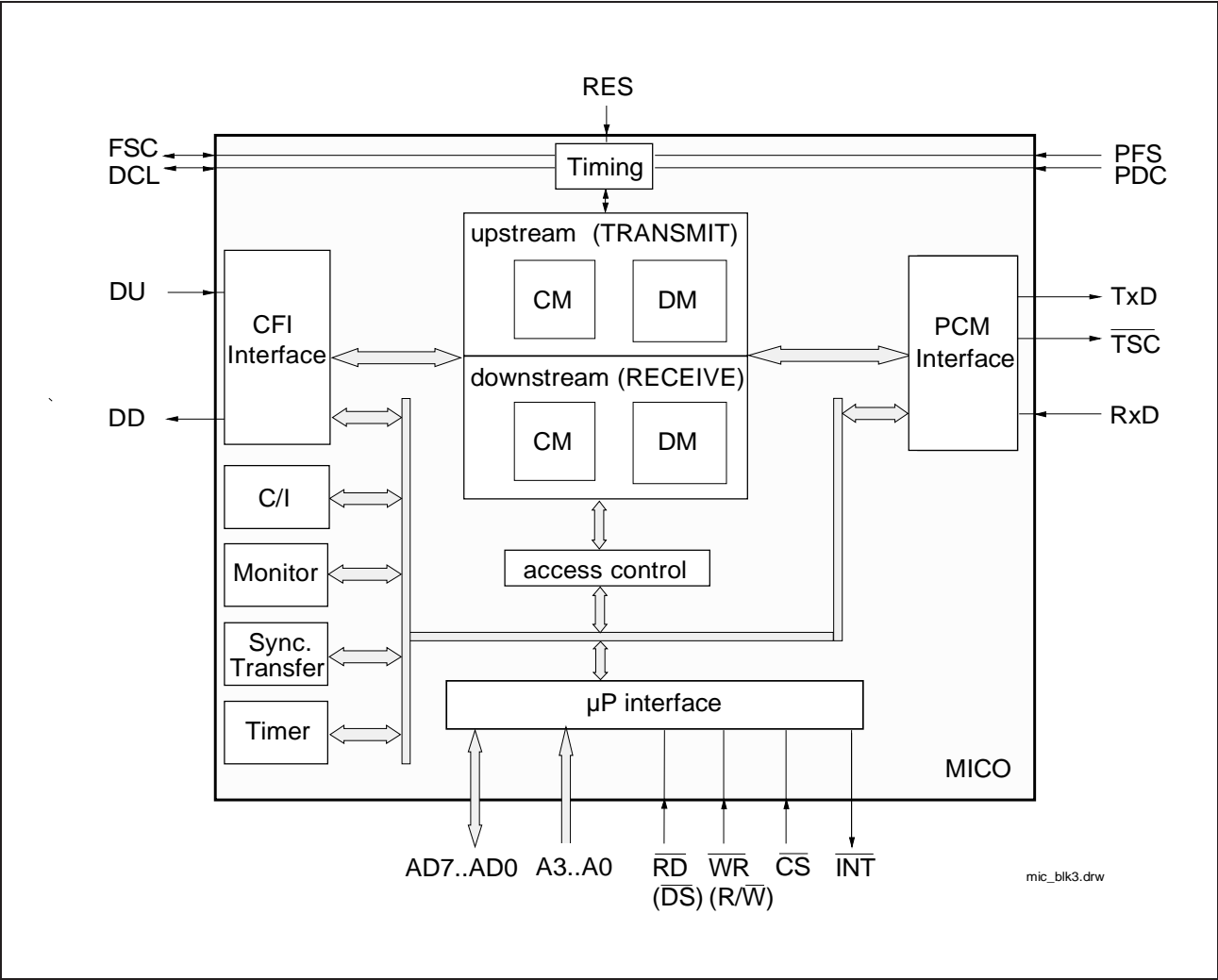


Figure 3
Functional Block Diagram

2 Functional Description

2.1 IOM-2 Interface

The integrated CFI is a one port serial interface. It comprises two serial data lines (upstream DU and downstream DD), a data clock input or output DCL and a frame sync input or output FSC in IOM-applications. The clock frequency is either equal to the data rate or twice the data rate. The CFI can be configured to data rates up to 8.192 Mbit/s.

The CFI is typically used in IOM-2 or SLD configuration to connect layer-1 devices.

Figure 4 shows the IOM-2 Interface structure in Line Card Mode:

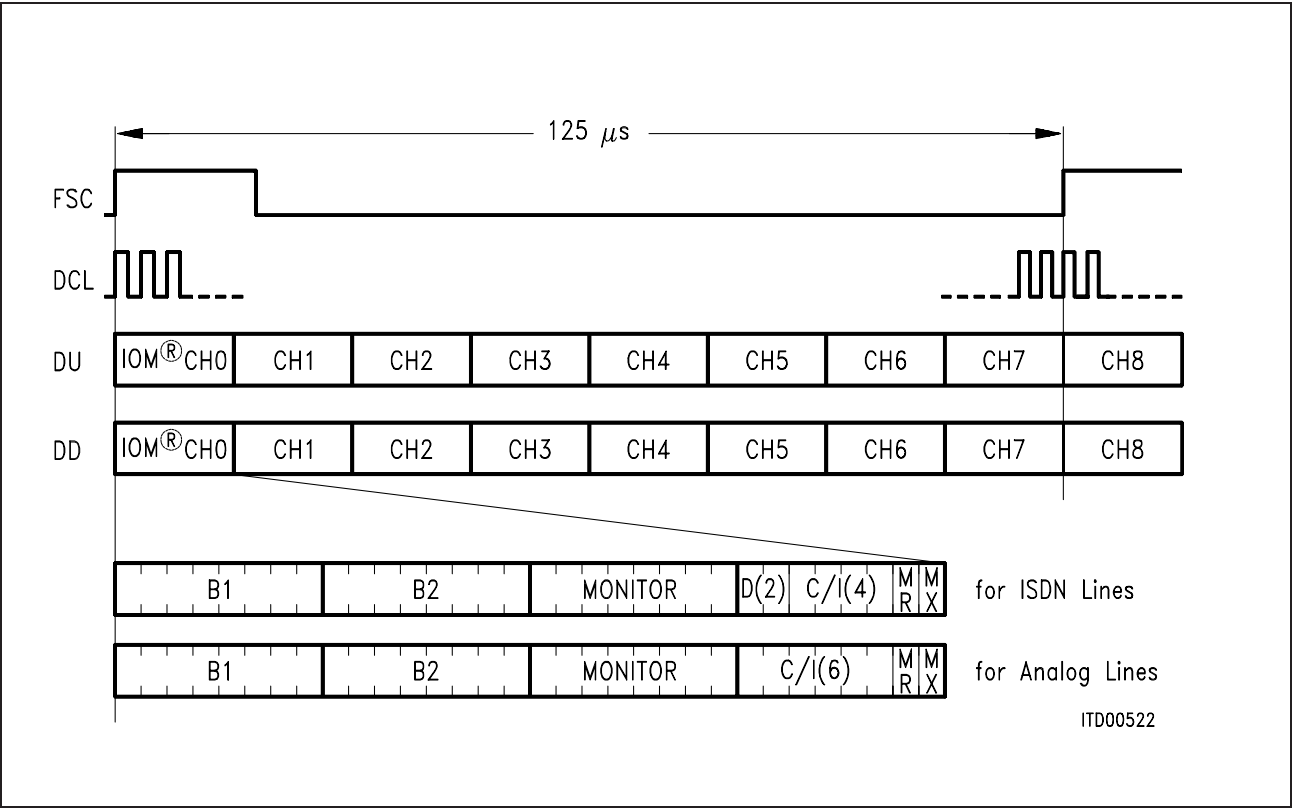


Figure 4
IOM-2 Frame Structure with 2.048 Mbit/s Data Rate

The MICO allows the access to all 32 time slots, i.e. 8 IOM-channels, within a frame. The device therefore can handle up to 8 ISDN subscribers or up to 16 analog subscribers (8 using the SLICOFI). Additionally the MICO contains a C/I- and MONITOR-handler to process the C/I- and MONITOR-channels of the IOM-2 protocol.

Functional Description

2.2 Serial PCM Interface

The PCM interface formats the data transmitted or received at the PCM-highways. It consists of one port comprising a data receive (RxD), a data transmit (TxD) and an output tristate indication line (\overline{TSC}). The PCM interface is supplied with a frame signal (PFS) and a PCM clock (PDC).

Data rates up to 8.192 Mbit/s are supported. To properly clock the PCM interface a PDC signal with a frequency equal or twice the data rate has to be applied to the MICO.

The IOM-2 time slots can be assigned to any of the PCM time slots and vice versa. Any PCM sub time slot can be switched to any of the 4 possible D-channel positions at the IOM-2 interface. In that way up to the 4 D-channels can be handled within one PCM time slot.

Figure 5 shows an example of switching 8 B-channels from the IOM-2 interface to 8 consecutive PCM time slots. Furthermore the 4 D-channels are concatenated and switched to the next PCM time slot after the B-channels.

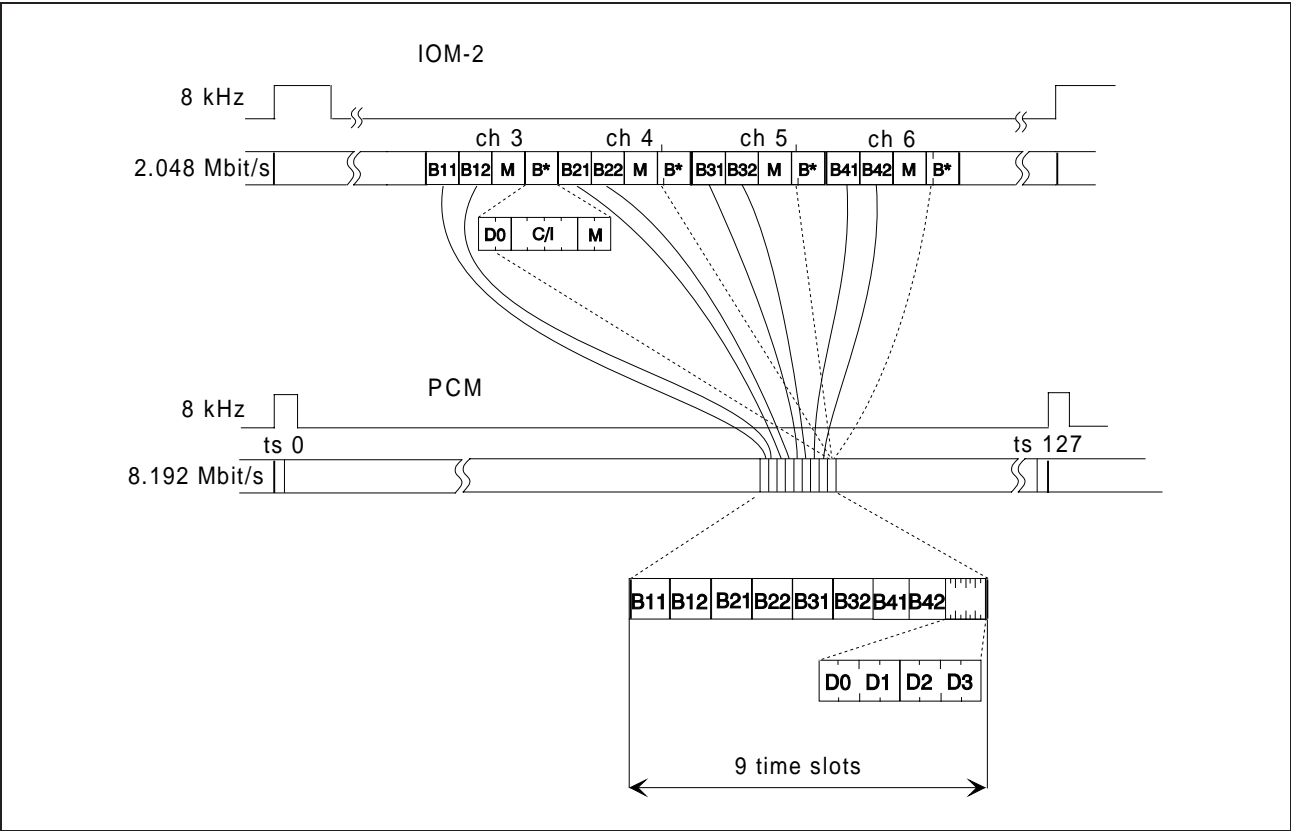


Figure 5
Example of Switching IOM-2 channels to consecutive PCM Time Slots

In principle every B-channel may be assigned to any PCM time slot. One D-channel may occupy a single PCM time slot as well.

Note: Frame delay is controlled by appropriate programming of switching paths (refer to EPIC User's Manual).

Functional Description

2.3 Microprocessor Interface

The MICO supports Siemens/Intel and Motorola type microprocessors. In the Siemens/Intel type μ P interface either a multiplexed or a demultiplexed bus structure may be chosen.

The interface type is selected by pulling up or down two address pins (A1, A0) during the reset state. Pulling-up the appropriate pins selects the Motorola type μ P interface, fixing them to ground chooses the Siemens/Intel type μ P interface mode. In case of a multiplexed Siemens/Intel bus structure address pin A0 takes over the ALE functionality.

The microprocessor interface consists of the following lines:

- Data Bus, 8-bit wide, D7..D0
- Address bus, 4-bit wide, A3..A0
- Chip select, \overline{CS}
- Two read/write control lines: \overline{RD} and \overline{WR} (Intel mode) or \overline{DS} and R/\overline{W} (Motorola mode)
- Interrupt, \overline{INT}
- Reset, RES

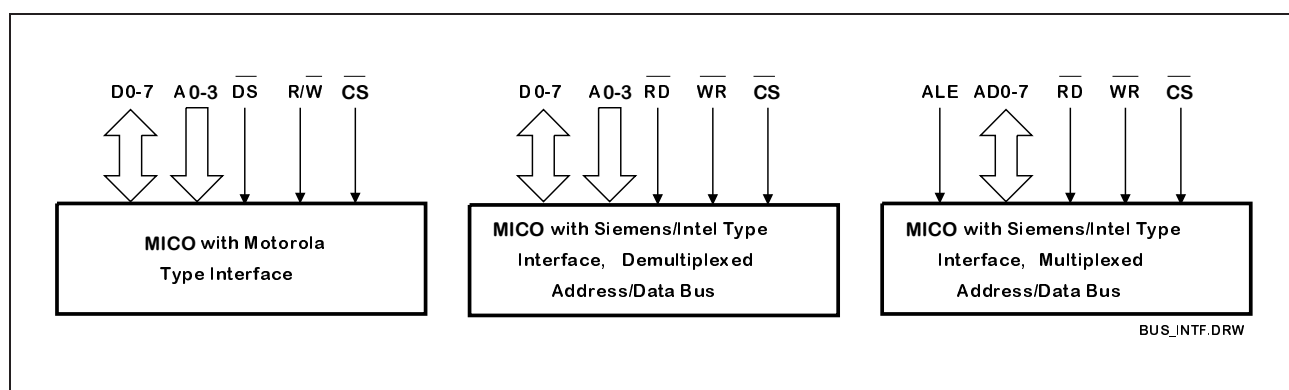


Figure 6
Selectable Bus Interface Structures

2.4 Special Functions

- Synchronous transfer.
This utility allows the synchronous μ P-access to two independent channels on the PCM- or CFI-interface. Interrupts are generated to indicate the appropriate access windows.
- 7-bit hardware timer.
The MICO offers one hardware timer. It can be used to cyclically interrupt the CPU, to determine the double last look period or to generate a proper CFI-multiframe synchronization signal.
- Frame length checking.
The PFS-period is internally checked against the programmed frame length.

3 Application Examples

3.1 Access Network

Access Networks are used in order to connect subscribers to the telecom network quickly and at low cost.

One possibility is to use the existing cable TV network to provide telephony services. An existing hybrid fiber-coaxial network (HFCN) that has been upgraded for upstream communication is the basis for such an Access Network. **Figure 7** illustrates the functional model of an optical access network (Fiber In The Loop FITL).

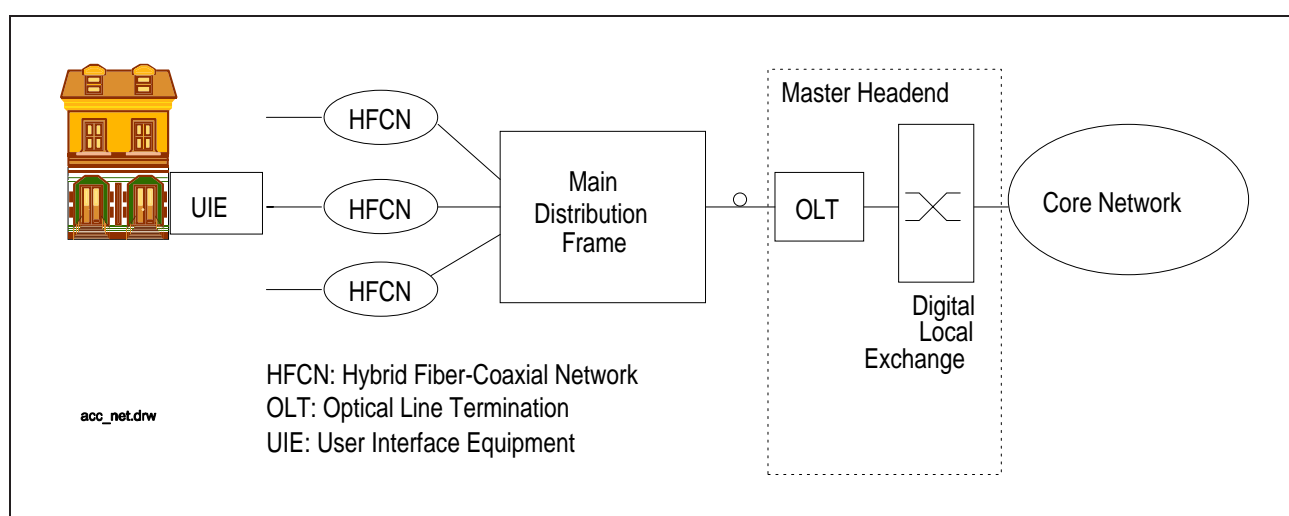


Figure 7
Functional Model of an Optical Access Network

The master headend will serve one or multiple main distribution frames. Via the HFCN the UIE is provided. Depending on the number of supported user ports and how far the fiber is available, the configuration is called Fiber To The Home (FTTH), Fiber To The Building (FTTB) or Fiber To The Curb (FTTC).

The MICO can be used in a configuration where a maximum of 16 POTS or 8ISDN subscribers are needed, e.g. FTTH or FTTB applications. **Figure 8** shows an example of an user interface equipment (UIE) providing two POTS and one ISDN subscriber.

Application Examples

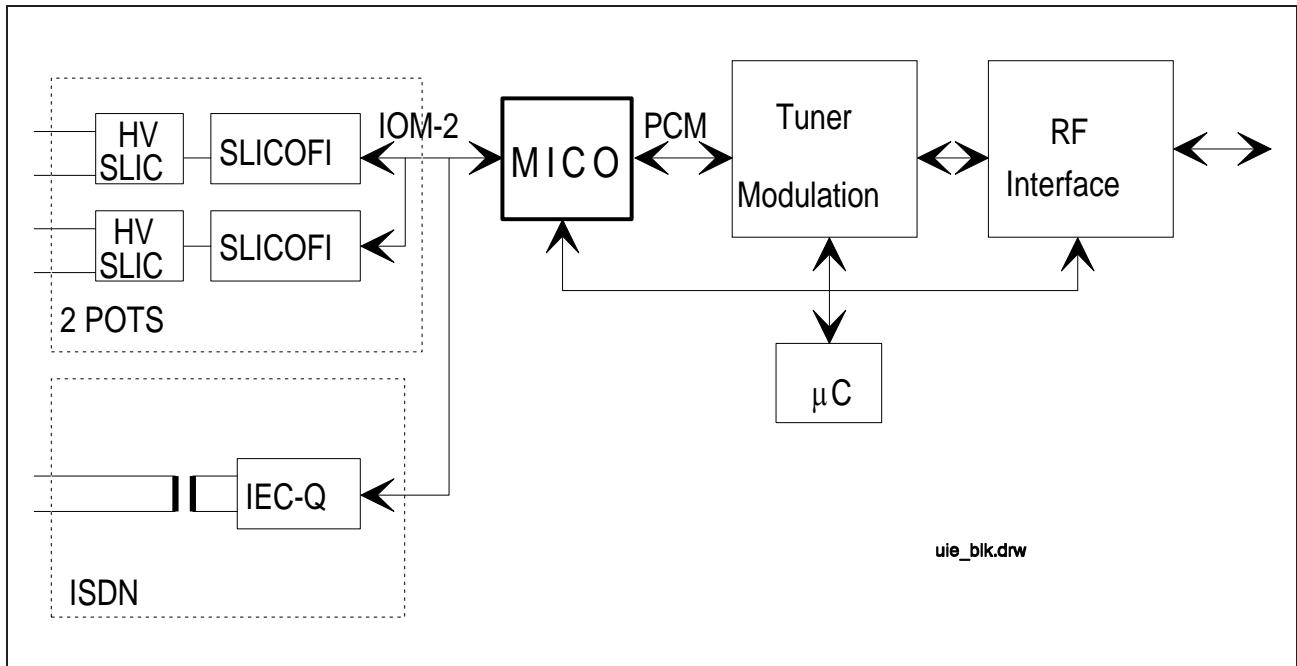


Figure 8
Example using the MICO in an UIE

The MICO will replace the EPIC in applications where only a few subscribers have to be supported. It connects the subscriber circuits to the HF unit providing switching capability. Additionally the subscriber circuits are controlled via the implemented C/I- and Monitor-Handlers.

3.2 Intelligent NT

An example of an Intelligent NT (network termination) using the MICO is shown in **figure 9**. This gives the ability to connect up to 16 analog (8 using the SLICOFI) subscribers via a t/r line to the NT. Switching functions within the NT are not supported. The PLL provides a 4.096 MHz clock required by the IOM-2 interface in Line Card Mode. This 4.096 MHz clock is derived from the available 1.536 MHz NT clock.

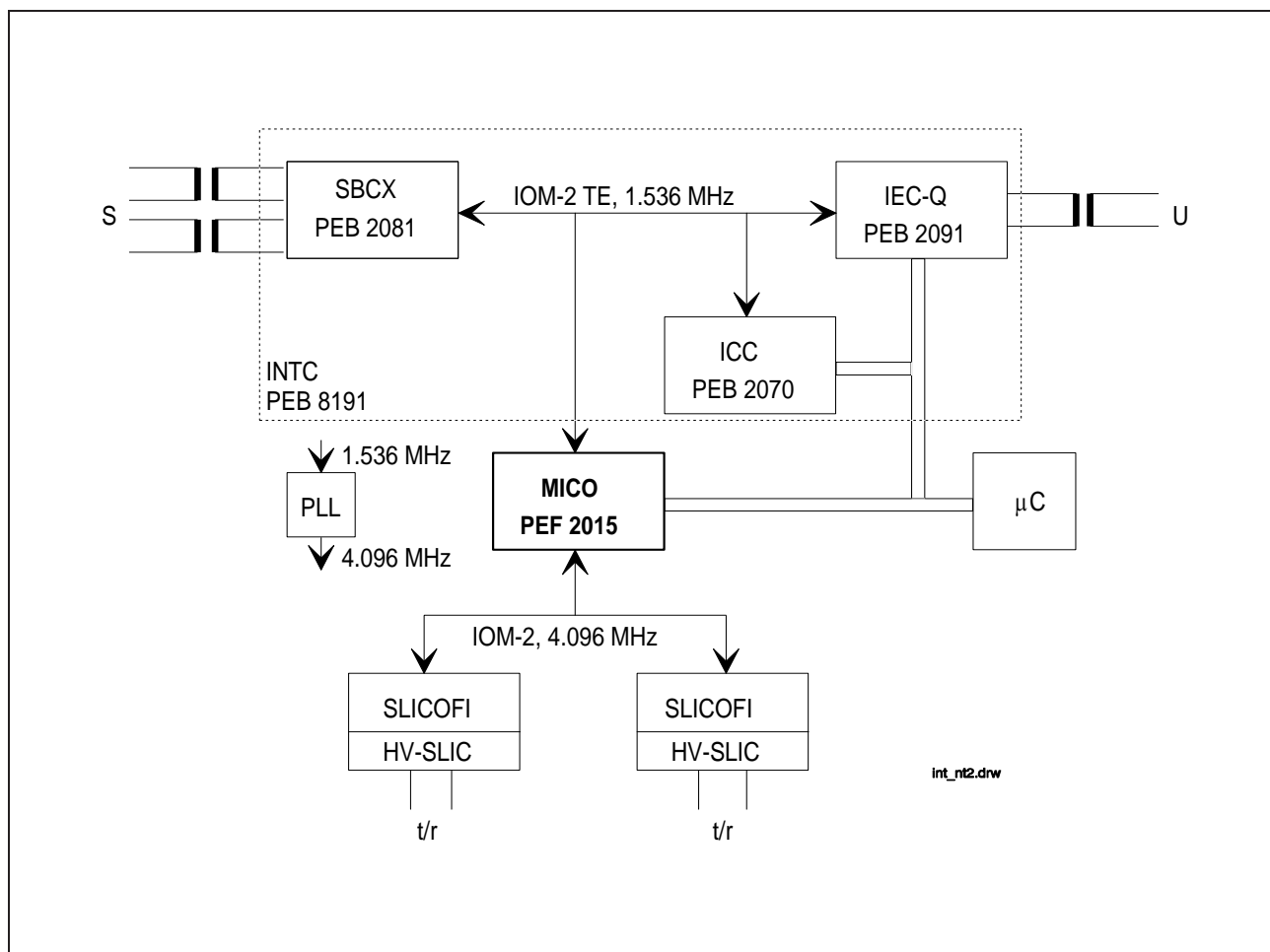


Figure 9
MICO with 2 SLICOFIs in an Intelligent NT

The MICO PCM port has to be configured according to the IOM-2 TE mode supplying a data rate of 768 kbit/s. This is the data rate used within the NT. **Figure 10** shows the IOM-2 TE mode frame structure.

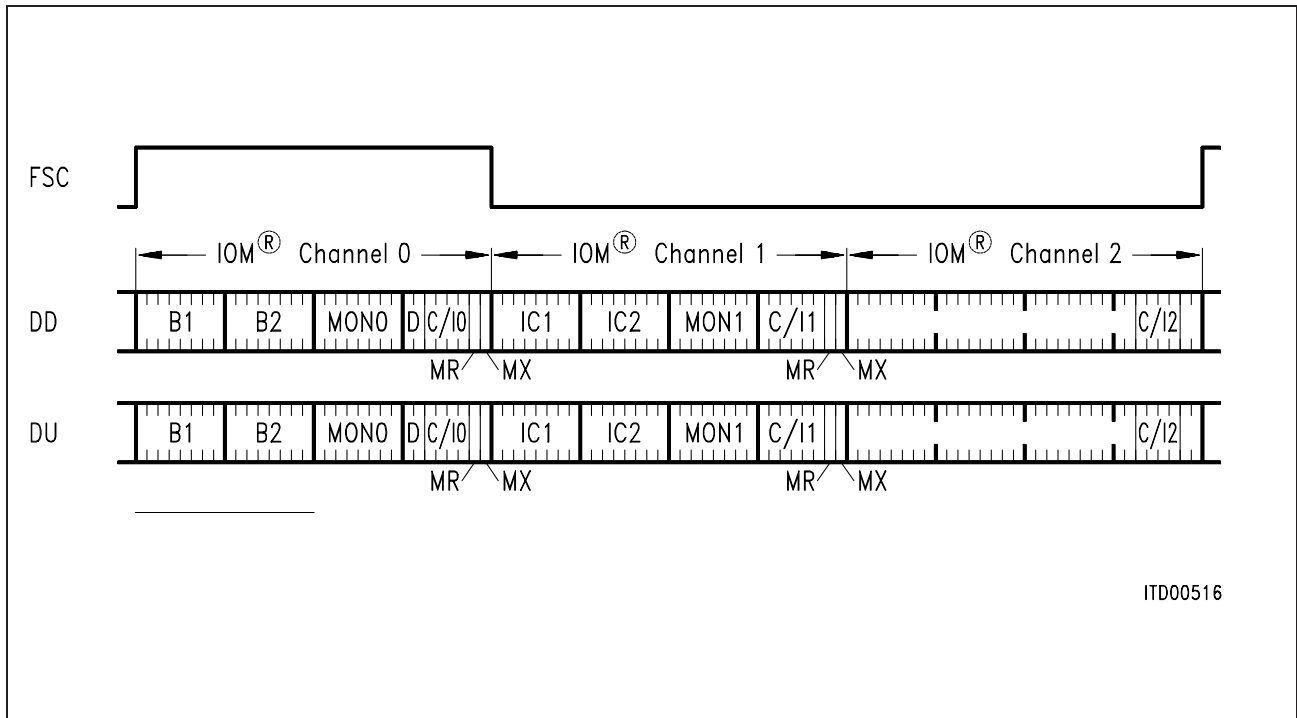


Figure 10 IOM-2 Terminal Mode Frame Structure

As the SLICOFIs are tied to the B1-channels two IOM-2 channels are needed on the IOM port. These have to be switched to the B1- or B2-channel at the PCM port configured as IOM TE mode. The possible time slot assignments are depicted in **figure 11**.

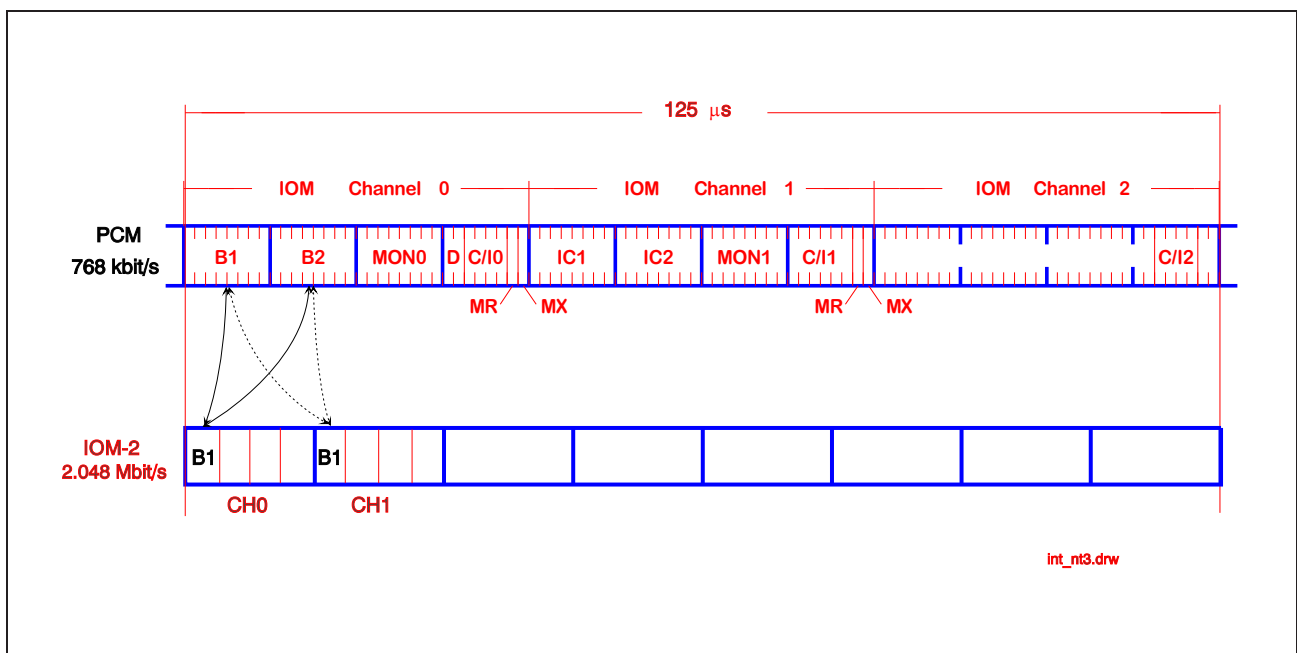
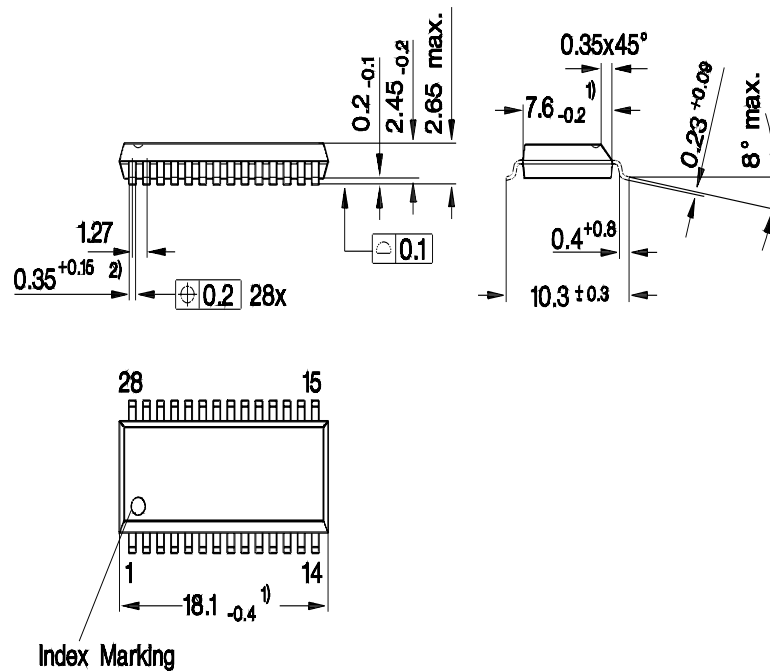


Figure 11
Time Slot Assignment in the Intelligent NT using the MICO with 2 SLICOFIs

4 Package Outlines

P-DSO-28

(Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm